

## PATENT ABSTRACTS OF JAPAN

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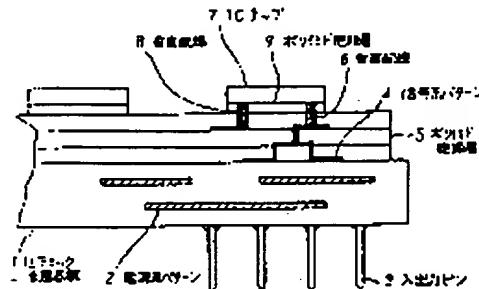
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## (54) MULTIPLE-CHIP PACKAGE

## (57) Abstract:

PURPOSE: To make it possible to perform highly reliable, high-density packaging, by directly connecting a ceramic multilayer substrate and an integrated circuit such as an IC or an LSI with a polyimide insulating layer and a vertical wiring.

CONSTITUTION: A ceramic multilayer substrate 1 is a multilayer circuit substrate, which includes a power source system pattern 2 comprising tungsten. Input/output pins 3 comprising a kovar material and the like are attached with silver solder to the lower surface. A polyimide insulating layer 5, in which a signal system pattern 4 is included, is formed on the upper surface as a multilayer form. The pattern 4 is selectively plated with gold, and formed in the insulating layer 5 through necessary via-holes in the multilayer shape. At the uppermost part of the insulating layer 5, a vertical wiring 6, which is connected to a pattern 4, is formed. Vertical wirings 8 are formed for a plurality of IC chips 7 so that the wirings 8 are connected to the wiring 6. A polyimide insulating layer 9 is formed beneath the IC chip 7 and contacted with the insulating layer 5. The insulating layer 5 and 9 are completely cured. The wirings 6 and 8 are bonded by thermal compression of gold-gold. Local pressure is not applied as shown in TAB connections. Since the contact is made with the surface of the insulating layer 9, there is no deformation or breakdown.



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